ABSTRACT OF THE DISCLOSURE

A C element controls a pipeline register and successively transfers data packets. When a dead-lock state occurs, a data packet in the pipeline register is erased by a master reset signal, a host transfer flag operating circuit overwrites a data packet in the pipeline register so that it has a host transfer flag at the "H" level, and thereafter, when the host transfer flag is detected in the subsequent stage, the data packet is transferred to the host.